CLAIMS

What is claimed is:

1. A system comprising:

a media access controller (MAC); and

a communication device comprising:

a media independent interface (MII) coupled to the MAC to at least one of transmit and receive data at a data rate;

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection; and

logic to vary the data rate based, a least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection.

2. The system of claim 1, wherein the system further comprises a switch fabric coupled to the MAC.

3. The system of claim 1, wherein the system further comprises a packet classification device coupled to the MAC.

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4. A device comprising:

a media independent interface (MII) to at least one of transmit and receive data at a data rate;

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection; and

logic to vary the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection.

5. The device of claim 4, wherein each data lane interface is associated with a first differential pair to transmit a serial data signal and a second differential pair to receive a serial data signal.

6. The device of claim 5, wherein the plurality of data lane interface are capable of transmitting data to and receiving data from a 10 gigabit attachment unit interface.

7. The device of claim 4, wherein the device further comprises:

a plurality of 8B10B decoders, each 8B10B decoder being associated with one of the data lane interfaces, each 8B10B decoder being capable of decoding one eight bit byte from a differential pair on first intervals of a first clock signal;

a receive state machine to provide a fixed length data signal to the MII on second intervals of a second clock signal; and

logic to vary the second intervals based upon a number of the data lane interfaces actively receiving serial data from the device-to-device interconnection.

8. The device of claim 4, wherein the device further comprises:

a transmit state machine to receive a fixed length data signal from the MII on first intervals of a first clock signal;

a plurality of 8B10B encoders, each 8B10B encoder being associated with one of the data lane interfaces, each 8B10B encoder being capable of encoding one eight bit byte of the fixed length data signal for transmission to a differential pair on first intervals of a first clock signal; and

logic to vary the second intervals based upon a number of the data lane interfaces actively transmitting serial data from to the device-to-device interconnection.

9. The device of claim 4, wherein the device-to-device interconnection comprises printed circuit board traces.

10. The device of claim 4, wherein the device-to-device interconnection comprises a cable.

11. A method comprising:

at least one of transmitting data to and receiving data from a media independent interface (MII) at a data rate;

at least one transmitting a serial data signal to and receiving a serial data signal from one or more data lanes in a device-to-device interconnection, each data lane being coupled to the MII by an associated data lane interface; and

varying the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection.

12. The method of claim 11, the method further comprising:

transmitting one or more serial data signals to the device-to-device interconnection in a first differential pair signal; and

receiving one more serial data signals from the device-to-device interconnection in a second differential pair signal.

13. The method of claim 12, the method further comprising transmitting data to and receiving data from a 10 gigabit attachment unit interface.

14. The method of claim 11, wherein the method further comprises:

at one or more data lane interfaces, receiving a serial data signal from the device to device interconnection;

decoding the serial data signal according to an 8B10B decoding scheme to provide an eight-bit byte on byte intervals;

providing a fixed length data signal to the MII on intervals of a clock signal having a frequency; and

varying the frequency of the clock signal based upon a number of the data lane interfaces actively receiving a serial data signal from the device-to-device interconnection.

15. The method of claim 11, wherein the method further comprises:

receiving a fixed length data signal from the MII on intervals of a clock signal having a frequency, the fixed length data signal having a plurality of eight-bit bytes;

encoding each eight-bit byte into a ten bit code group according to an 8B10B encoding scheme;

transmitting the code groups to the device-to-device interconnection through one or more data lane interfaces; and

varying the frequency of the clock signal based, at least in part, upon a number of data lane interfaces actively transmitting serial data to the device-to-device interconnection.

16. The method of claim 11, wherein the device-to-device interconnection comprises printed circuit board traces.

17. The method of claim 11, wherein the device-to-device interconnection comprises a cable.

18. A system comprising:

a physical layer communication device to transmit data between a transmission medium and a media independent interface (MII) at a data rate; and

a communication device comprising:

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection; and

logic to vary the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection.

19. The system of claim 18, wherein the physical layer communication device is adapted to transmit data between the MII and a fiber optic cable.

20. The system of claim 20, wherein the physical layer communication device is adapted to transmit data between the MII and a twisted wire pair cable.

21. A device comprising:

a state machine to at least one of transmit and receive data at a data rate;

a plurality of data lane interfaces, each data lane interface being capable of at least one of transmitting a serial data signal to and receiving a serial data signal from a data lane in a device-to-device interconnection; and

logic to vary the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or actively receiving a serial data signal from the device-to-device interconnection.

22. The device of claim 21, wherein each data lane interface is associated with a first differential pair to transmit a serial data signal and a second differential pair to receive a serial data signal.

23. The device of claim 22, wherein the plurality of data lane interface are capable of transmitting data to and receiving data from a 10 gigabit attachment unit interface.

24. The device of claim 21, wherein the data rate is controlled by a frequency of a first clock signal, and wherein the device further comprises:

a plurality of 8B10B decoders, each 8B10B decoder being associated with one of the data lane interfaces, each 8B10B decoder being capable of decoding one eight bit byte from a differential pair at a rate controlled by a frequency of a second clock signal; and

logic to vary the frequency of the first clock signal based, at least in part, upon a number of the data lane interfaces actively receiving serial data from the device-to-device interconnection.

25. The device of claim 21, wherein the data rate is controlled by a frequency of a first clock signal, and wherein the device further comprises:

a plurality of 8B10B encoders, each 8B10B encoder being associated with one of the data lane interfaces, each 8B10B encoder being capable of encoding one eight bit

byte of the fixed length data signal for transmission to a differential pair at a rate controlled by a second clock signal; and

logic to vary the frequency of the first clock signal based, at least in part, upon a number of the data lane interfaces actively transmitting serial data from to the device-to-device interconnection.

26. The device of claim 21, wherein the device further comprises a MAC to at least one of transmit data to and receive data from the state machine at the data rate.

27. The device of claim 21, wherein the device further comprises a physical layer communication device to at least one of transmit data to and receive data from the state machine at the data rate.

28. The device of claim 21, wherein the device-to-device interconnection comprises printed circuit board traces.

29. The method of claim 21, wherein the device-to-device interconnection comprises a cable.

30. A method comprising:

at least one of transmitting data to and receiving data from a state machine at a data rate;

at least one transmitting a serial data signal to and receiving a serial data signal from one or more data lanes in a device-to-device interconnection, each data lane being coupled to the state machine by an associated data lane interface; and

varying the data rate based, at least in part, upon a number of the data lane interfaces actively transmitting a serial data signal to or receiving a serial data signal from the device-to-device interconnection.

31. The method of claim 30, the method further comprising:

transmitting one or more serial data signals to the device-to-device interconnection in a first differential pair signal; and

receiving one more serial data signals from the device-to-device interconnection in a second differential pair signal.

32. The method of claim 31, the method further comprising transmitting data to and receiving data from a 10 gigabit attachment unit interface.

33. The method of claim 30, wherein the device further comprises:

controlling the data rate according to a frequency of a clock signal;

at one or more data lane interfaces, receiving a serial data signal from the device to device interconnection;

decoding the serial data signal according to an 8B10B decoding scheme to provide an eight-bit byte on byte intervals; and

varying the frequency of the clock signal based upon a number of the data lane interfaces actively receiving a serial data signal from the device-to-device interconnection.

34. The method of claim 30, wherein the method further comprises:

receiving a fixed length data signal at the state machine at a rate controlled by a clock signal having a frequency, the fixed length data signal having a plurality of eight-bit bytes;

encoding each eight-bit byte into a ten bit code group according to an 8B10B encoding scheme;

transmitting the code groups to the device-to-device interconnection through one or more data lane interfaces; and

varying the frequency of the clock signal based, at least in part, upon a number of data lane interfaces actively transmitting serial data to the device-to-device interconnection.